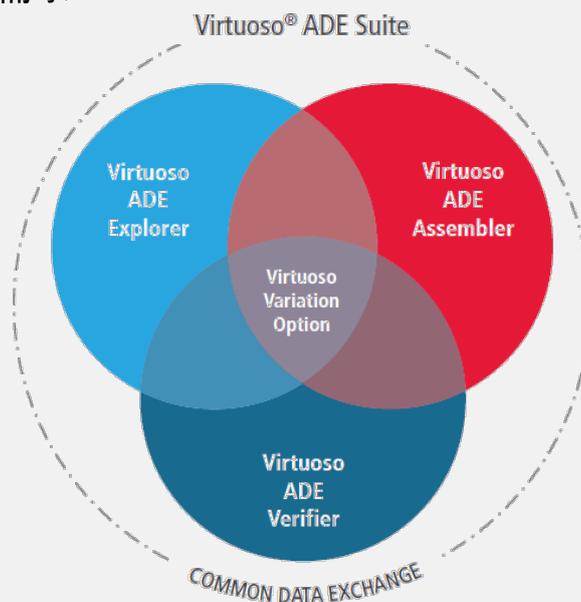


全新的類比設計環境 - Cadence Virtuoso ADE Product Suite

Cadence發表了新一代的類比設計環境，可為設計人員帶來**10倍跨平台效能與容量提升**，且新一代的Cadence® Virtuoso® ADE Product Suite 能夠克服新的業界標準、先進節點設計以及系統設計需求興起帶來的挑戰，協助工程師充分地探索、分析與驗證設計，以確保在整個設計周期中都能維持設計意圖，因應汽車安全、醫療裝置與物聯網(IoT)應用等需求。



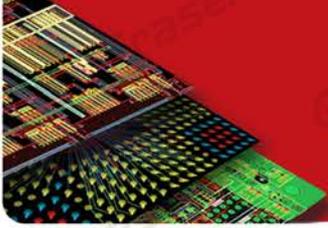
• **Date** : 2016 / 9 / 12

• **Author** : Scott

• **Revision** : 1.2

• **Version** : IC6.1.7

• **備註**:



Cadence® Virtuoso® ADE Explorer

實現快速、準確的設計規格即時調整，且可以依照使用者訂定的規格條件提示 Pass/Fail 的狀態，此外也提供完整的 Corner 與 Monte Carlo 統計環境，協助使用者偵測和修補變異性等問題，達到縮短設計時程的優勢。

Familiar ADE L menus

Design Window is opened in a tab

Define analysis, variables, corners, Monte Carlo directly in the Setup Assistant

Corners and Monte Carlo previously available only in the higher tiers

Name	Type	Details	Value	Plot	Save	Spec
/I/O/M1	oppoint	/I/O/M1 vdsat				
	signal	/OUT				
Swing	expr	(value(VT("/OUT") 2.5e-08) - val...	1.136			> 0.98
SettlingTime	expr	settlingTime(VT("/OUT") 0 t 2.5...	7.565 ns			< 8n
RelativeSwingPercent	expr	((Swing / VAR("vdd")) * 100)	75.73 %			> 75
PhaseMargin	expr	getData("/phaseMargin" ?result...	18.69 degree			> 20
	signal	/I/O/net6				
	signal	/I/O/net10				
vdsat	expr	OT("/I/O/M1" "vdsat")				

- Results are shown in the Value column for single point simulations (ADE L style)
- For multi-point simulations a Results tab opens (ADE XL style)
- Color coded specifications for easy visualization of design status

"Familiar" ADE L toolbar

Cadence® Virtuoso® ADE Explorer cockpit

Monte Carlo Setup

Statistical Variation: Process, Mismatch, All

Sampling Method: Low-Discrepancy Sequence

Max Number of Points: 88

Target Yield: 94 %

Probability (1-alpha): 95.8 %

Output Setup

Test	Name	Yield	Min	Target	Max	Mean	Std Dev
TRN	Swing	100	1.131	> 980m	1.141	1.136	2.747m
	Swing	100	1.131		1.141	1.136	2.747m
	SettingTime	100	7.485 ns	< 8n	7.648 ns	7.566 ns	42.46 ps
	SettingTime	100	7.485 ns		7.648 ns	7.566 ns	42.46 ps
	RelativeSw...	100	75.43 %		76.1 %	75.75 %	183.1 m%
	RelativeSw...	100	75.43 %		76.1 %	75.75 %	183.1 m%
	PhaseMa...	0	17.77 degree	> 20	19.32 degree	18.61 degree	454.6 mdegree
	PhaseMa...	0	17.77 degree		19.32 degree	18.61 degree	454.6 mdegree

WVA Graph

SettingTime

Pass = 26/20 (100%)

Mean = 7.56641n

Std Dev = 42.4551p

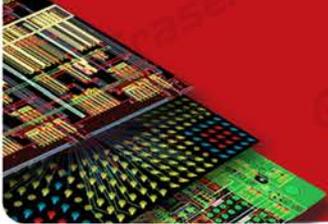
normalQQ(SettingTime)

Normal

r = 0.9889

p = 0.9138

Monte Carlo analysis



Design Variables

M6_M8_finger_ratio	2
M6_M7_finger_ratio	4
M10_M9_finger_ratio	2
vdd	1.8

Parameters

M1/l	300n
M1/w	120u
NM0/l	300n
NM0/fw	12u

Slider bar: 900m to 2.7

Annotations:

- Design Variables section that lists all the design variables and their values defined in the Setup
- Parameters section that lists all the parameters and their values defined in the Setup
- Stop simulation button to stop running simulation after a value is changed.
- Undo button to bring back the changed variable and parameter values to the previous values
- Play button to put the simulator into listening mode
- Redo button to bring back the changes. It works in synchronization with the Undo button.
- Load button to load the design and variable values from the original setup
- Save button to save the updated values back into the Explorer setup
- Slider bar that you can use to dynamically change the values of variables and parameters. When these values are modified, the output results are simultaneously updated in the graph window.

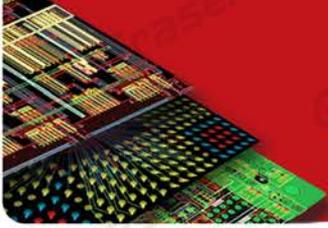
Real-Time Tuning in Simulations

Outputs only

Outputs with docked ViVA

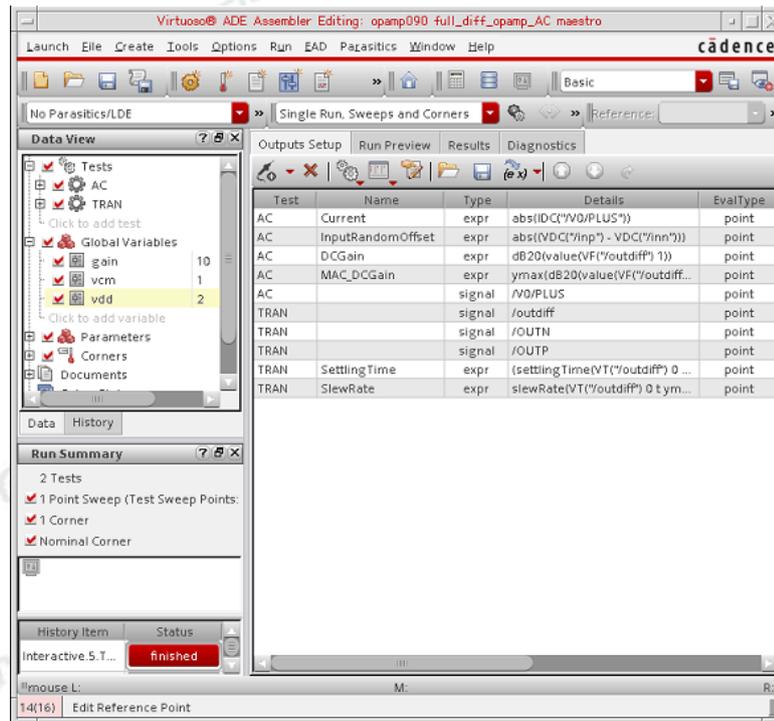
Schematic with waveform balloons and docked ViVA

Variety of waveform displays



Cadence® Virtuoso® ADE Assembler

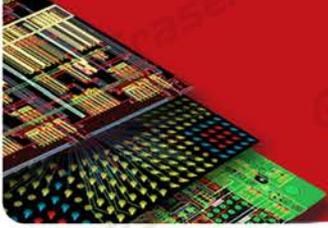
協助工程師在不同的製程—電壓—溫度(PVT) 組合條件分析其設計，並提供基於 GUI 的驗證計畫，因此設計人員能輕鬆地建立條件與相依性模擬。



Cadence® Virtuoso® ADE Assembler cockpit

Point	Corner	VDD	fclk	gpdck045.sc	temperature	Pass/Fail	tau_m	Probability of Error
1	C1_1	1.2	100M	mc	80	fail	8.89p	0
2	C1_2	1.2	100M	mc	120	fail	9.96p	0
3	C1_1	1.2	110M	mc	80	fail	8.811p	0
4	C1_1	1.2	120M	mc	80	fail	8.879p	0
5	C1_1	1.2	130M	mc	80	fail	8.873p	0
6	C1_1	1.2	140M	mc	80	fail	8.908p	0
7	C1_2	1.2	140M	mc	120	fail	9.923p	495.2e-312

Filtering of results



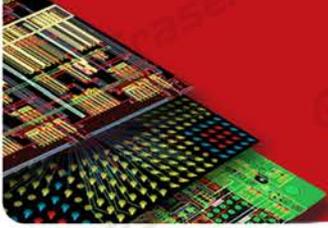
Copy of the active setup (2 tests at Nominal)

Copy of the active setup with modification (Monte Carlo run on 1 test)

Run that is equal to active setup but VDD=3V

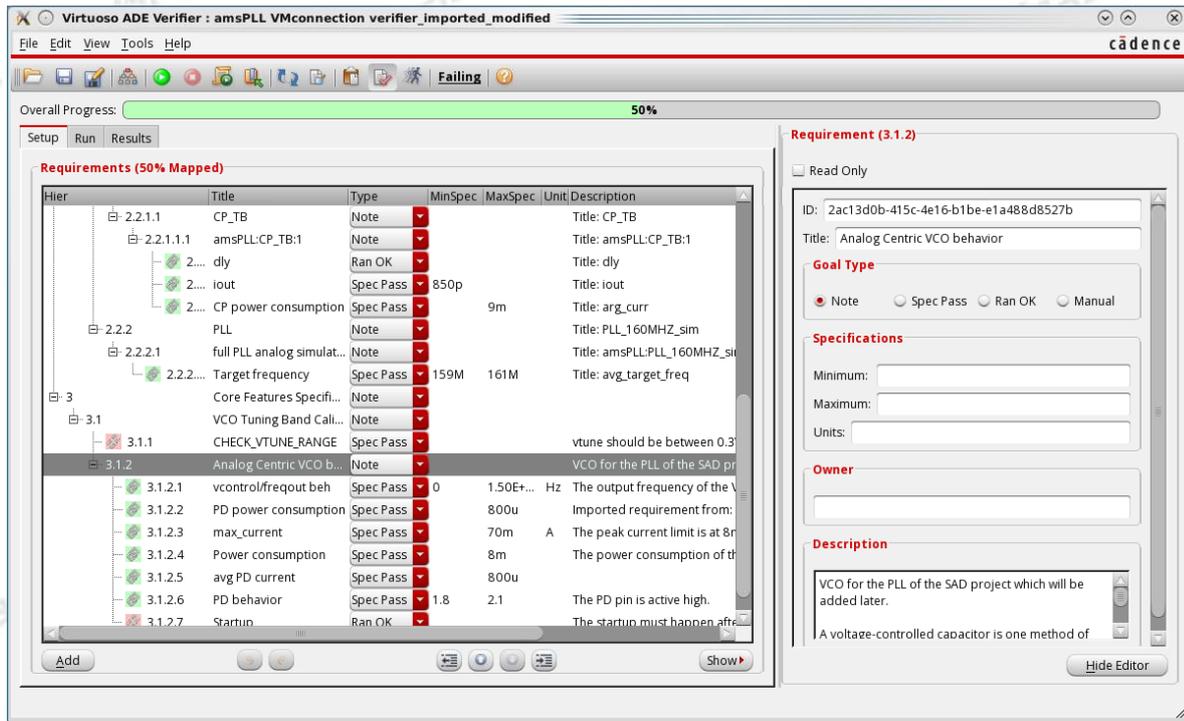
Run Plan

Run Plan

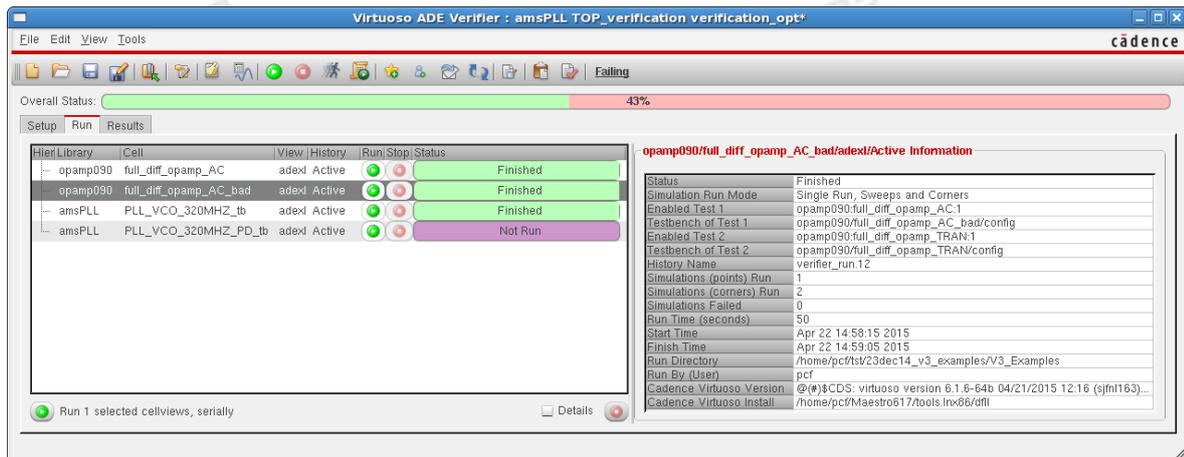


Cadence® Virtuoso® ADE Verifier

提供一個整合式驗證環境，可讓工程師/產品經理輕鬆連結到與設計有關的所有模塊去進行驗證與分析，進而掌控各模塊的執行進度以執行最佳資源分配。



Cadence® Virtuoso® ADE Verifier cockpit



Cadence® Virtuoso® ADE Verifier job monitor

